**IN THE CLAIMS**

Please cancel claims 17-24.

1. (Original) A semiconductor integrated circuit device, comprising:

a semiconductor substrate squared in plane surface;

a plurality of pads disposed over a main surface of the semiconductor substrate along one side of the semiconductor substrate;

a plurality of input/output cells disposed corresponding to the plural pads over the main surface of the semiconductor substrate;

an internal circuit forming section disposed over the main surface of the semiconductor substrate and inner than the plural input/output cells; and

power supply wirings for internal circuit, for supplying potentials to the internal circuit forming section, said power supply wirings being respectively disposed inner than the plural input/output cells,

wherein the plural input/output cells include signal cells and power supply cells for internal circuit respectively,

wherein the plural pads includes signal pads respectively disposed corresponding to the signal cells and electrically connected the signal cells, and power supply pads for internal circuit respectively disposed corresponding to the power

supply cells and electrically connected to the power supply cells and the power supply wirings, and

wherein the power supply pads are disposed closer to the power supply wirings than the signal pads.

2. (Original) The semiconductor integrated circuit device according to claim 1, wherein the power supply pads are respectively disposed inner than the input/output cells respectively.

3. (Original) The semiconductor integrated circuit device according to claim 1, wherein the power supply pads are respectively disposed so as to overlap with the power supply wirings in a plane manner.

4. (Original) The semiconductor integrated circuit device according to claim 1, wherein the signal pads are respectively disposed outer than the input/output cells.

5. (Original) The semiconductor integrated circuit device according to claim 1, wherein the signal pads are respectively disposed inner than outer ends of the input/output cells.

6. (Original) The semiconductor integrated circuit device according to claim 1, wherein the power supply wirings are disposed outer than the internal circuit forming section.

7. (Original) The semiconductor integrated circuit device according to claim 1, wherein the power supply wirings extend so as to surround the internal circuit forming section.

8. (Original) The semiconductor integrated circuit device according to claim 1,

wherein each of the signal cells includes a logic area in which input/output circuits are provided, and a final stage area in which a protective circuit is provided, and

wherein the logic area is disposed on one side of the semiconductor substrate rather than the final stage area.

9. (Original) A semiconductor integrated circuit device, comprising:

a semiconductor substrate squared in plane surface;

a plurality of pads disposed over a main surface of the semiconductor substrate along one side of the semiconductor substrate;

a plurality of input/output cells disposed corresponding to the plural pads over the main surface of the semiconductor substrate;

an internal circuit forming section disposed over the main surface of the semiconductor substrate and inner than the plural input/output cells;

power supply wirings for internal circuit, for supplying potentials to the internal circuit forming section, said power supply wirings being respectively disposed inner than the plural input/output cells; and

power supply wirings for input/output cells, for respectively supplying potentials to the plural input/output cells, said power supply wirings extending along one side of the semiconductor substrate so as to overlap with the plural input/output cells in a plane manner,

wherein the plural input/output cells include signal cells, power supply cells for internal circuit, and power supply cells for input/output cells respectively,

wherein the plural pads respectively include signal pads disposed corresponding to the signal cells and electrically connected to the signal cells, power supply pads for internal circuit respectively disposed corresponding to the power supply cells for internal circuit and electrically connected to the power supply cells for internal circuit and the power supply wirings for internal circuit, and power supply pads for input/output cells respectively disposed corresponding to the power supply cells for input/output cells and electrically connected to the power supply cells for input/output cells and the power supply wirings for input/output cells, and

wherein the power supply pads for internal circuit are disposed closer to the power supply wirings for internal circuit than the signal pads.

10. (Original) The semiconductor integrated circuit device according to claim 9, wherein the power supply pads for internal circuit are respectively disposed inner than the input/output cells.

11. (Original) The semiconductor integrated circuit device according to claim 9, wherein the power supply pads for internal circuit are respectively disposed so as to overlap with the power supply wirings for internal circuit in a plane manner.

12. (Original) The semiconductor integrated circuit device according to claim 9, wherein the signal pads and the power supply pads for input/output cells are respectively disposed outer than the input/output cells.

13. (Original) The semiconductor integrated circuit device according to claim 9,

wherein the signal pads are respectively disposed so as to overlap with the input/output cells in a plane manner, and

wherein the power supply pads for input/output cells are respectively disposed so as to overlap with the power supply cells for input/output cells in a plane manner.

14. (Original) The semiconductor integrated circuit device according to claim 9, wherein the power supply wirings for internal circuit are disposed outer than the internal circuit forming section.

15. (Original) The semiconductor integrated circuit device according to claim 9, wherein the power supply wirings for internal circuit extend so as to surround the periphery of the internal circuit forming section.

16. (Original) The semiconductor integrated circuit device according to claim 9,

wherein each of the signal cells includes a logic area in which input/output circuits are provided, and a final stage area in which a protective circuit is provided, and

wherein the logic area is disposed on one side of the semiconductor substrate rather than the final stage area.

17. (Canceled).

18. (Canceled).

19. (Canceled).

20. (Canceled).

21. (Canceled).

22. (Canceled).

23. (Canceled).

24. (Canceled).